

CLAIMS

What is claimed is:

- 1 SUB
2 BI } of:
3 1. A method for fabricating a memory device, the method comprising the steps
4 (a) providing a portion of a dual gate oxide in a periphery area of the memory
5 device;
6 (b) simultaneously providing a dual gate oxide in a core area of the memory
7 device and completing the dual gate oxide in the periphery area; and
8 (c) providing a nitridation process in both the core area and periphery area of the
memory device subsequent to steps (a) and (b).

- 1 2. The method of claim 1 further comprising:
2 (d) depositing a layer of type-1 polysilicon in both the core area and periphery
3 area of the memory device;
4 (e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon;
5 and
6 (f) removing the layer of oxide nitride oxide and a portion of the layer of type-1
7 polysilicon from the periphery area of the memory device.

- 1 3. The method of claim 2 wherein step (f) further includes removing
2 approximately half the layer of type-1 polysilicon from the periphery area of the memory
3 device.

1 4. The method of claim 3 further comprising:
2 (g) depositing a layer of type-2 polysilicon in both the core and periphery areas of
3 the memory area.

1 5. A flash memory device, comprising;
2 a core area having a plurality of memory transistors comprising an oxide layer, a first
3 poly layer, an interpoly dielectric layer, and a second poly layer; and
4 a periphery area having a plurality of transistors comprising an oxide layer, a portion
5 of the first poly layer, and the second poly layer.

1 6. The flash memory device of claim 5 wherein the interpoly dielectric layer
2 comprises oxide nitride oxide.

1 7. The flash memory device of claim 6 wherein the portion of the first poly
2 layer in the periphery area comprises one half the first poly layer in the core area.

1 8. The flash memory device of claim 7 wherein the first poly layer comprises a
2 type-1 polysilicon.

1 9. The flash memory device of claim 8 wherein the second poly layer comprises
2 a type-2 polysilicon.

1 SUB 10. A method for fabricating a memory device, the method comprising the steps
2 B2

2 of:

3 (a) providing a portion of a dual gate oxide in a periphery area of the memory
4 device;

5 (b) simultaneously providing a dual gate oxide in a core area of the memory
6 device and completing the dual gate oxide in the periphery area;

7 (c) providing a nitridation process in both the core area and periphery area of the
8 memory device subsequent to steps (a) and (b);

9 (d) depositing a layer of type-1 polysilicon in both the core area and periphery
10 area of the memory device;

11 (e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon;
12 and

13 (f) removing the layer of oxide nitride oxide and a portion of the layer of type-1
14 polysilicon from the periphery area of the memory device.

15 11. The method of claim 10 wherein step (f) further includes removing
16 approximately half the layer of type-1 polysilicon from the periphery area of the memory
17 device.

18 12. The method of claim 11 further comprising:

19 (g) depositing a layer of type-2 polysilicon in both the core and periphery areas of
20 the memory area.

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